REDUNDANCY SCHEME FOR A MEMORY ARRAY

Abstract of Disclosure

An IC with a memory array comprises a redundancy unit. The redundancy unit includes a tag portion, an address portion, and a redundant memory cell portion. A comparator determines whether an address of a read or a write command matches with the address stored in the address portion of the redundancy unit and switches from the normal data path to the memory cell portion of the redundancy unit.

Figures